ABSTRACT

This paper describes the world’s smallest SVGA (800x600) and WVGA (854x480) microdisplay that enables high-resolution images in ultra-portable products. The device uses Liquid Crystal on Silicon (LCOS) technology, supports single panel field sequential color operation, has a 5.4-micron pixel pitch, and is less than 7mm tall.

1. INTRODUCTION

Pico-projectors are extremely small projectors that will be integrated into all forms of ultra-portable mobile devices such as cell phones, personal media players, and cameras. Pico-projectors are also the one area of display projection technology that is anticipated to have explosive growth over the next 3 years. The challenge with pico-projection display devices is to meet the size, cost, power and resolution requirements of ultra-portable applications.

While there has been a significant degree of media attention paid to pico-projectors, prior to this device, this is the first device to demonstrated SVGA and WVGA resolution with a microdisplay that is less than 7mm tall. Moreover, while two dimensional laser beam steering systems have claimed similar resolutions, to date they have been unable to demonstrate their claimed resolution.

Just as computer displays, television, and digital cameras have increased in resolution, pico-projectors will soon be expected to support higher resolution [1]. Figure 1 shows our LCOS microdisplay designed for Pico-Projector market. It has 854x600 pixels. Figure 2 shows picture take of an image projected by the device. The architecture behind this microdisplay will be scaled to higher resolutions including but not limited to 1280x800 pixels.

2. Challenges to Making a Field Sequential LCOS for Pico-Projectors

Meeting the size, power, and cost requirements for a pico-projector microdisplay requires the use of field sequential color. Field sequential color has long been used with LCOS for near-eye applications, but near eye applications project the light directly into the eye and do not have the light-on-time duty cycle requirements of front projectors. They generally have lower resolution and relatively large pixel sizes. It turns out that designing a microdisplay for a “pico-projector” presents a number of significant challenges.

LCOS has also been used in the past for field sequential rear projection TV (RPTV) applications with rotating color wheels or the like to raster/scroll the change in color across the display device [2]. The display device could be updated gradually line by line ahead of the rastering of the color.

LED and laser field sequential color illuminates the entire display simultaneously, what we call “Flash Sequential Color” which obsoletes most prior LCOS display drive methods discussed above.
as it creates a whole set of new and unique drive requirements and challenges as discussed below.

2.1 Small Pixel Size
The first challenge to designing a small form-factor microdisplay for pico-projection is to design a small pixel while supporting field sequential color. The LC material requires a relatively high voltage of 5V, which in turn means there can be very few transistors under the pixel mirror. We use a simple high voltage six-transistor SRAM bit under each display mirror/pixel. We call the high voltage SRAM under the mirror the Mirror-RAM or MRAM.

Another approach to dealing with Flash Field Sequential Color requires an Analog “master slave” or double buffer under each pixel [3]. The high voltages, size of the multiple capacitors, and sensitivity of the analog circuitry results in a much larger pixel size than the 5.4 µm we have achieved with a digital pixel.

2.2 Small Packaged Device Size
Critical to making a small device is to reduce the peripheral circuitry and number of data pins. We used a very small Single Instruction Multiple Data stream (SIMD) processor with a processing element (PE) for each column of pixels to control the pulse widths that drive each pixel as shown in the block diagram in Figure 3. This architecture is based off an earlier architecture we developed for RPTVs [4].

The SIMD processor uses a small amount of dense scratch SRAM memory in the periphery. The PEs and SRAM are small enough that they fit in the glue gasket/seal used in assembling the LCOS device.

By having on-display processing, we are able to send encoded data that is decoded by the SIMD processor. This lowers the bandwidth and thus the number of data pins which allow the I/O to bond out on the short side of the device which helps maintain the critical package height of less than 7 mm.

2.3 Support “Flash Sequential Color” with high percentage of Light-On-Time
To provide the maximum light on-time most effectively use light sources, the time between color fields when the light is off needs to be minimized. There are two key parts to this issue A) the liquid crystal characteristics and B) the time to change the drive from one color to the next.

The switching speed, particularly the fall time, of the liquid crystal is critical to provide good light-on-time and color saturation. We use a fast switching twisted nematic LC that has a fall time on the order of 200 microseconds and a rise time on the order of 600 microseconds. Others have tried using VAN LC which has a much slower switching response that will result in significantly less light-on-time and/or poor color saturation.

Ferroelectric LC (FLC) has also been tried but requires the light to be off for over 50% of the time due to DC balancing requirement of FLC.

What we call the “color context switch” occurs each time the color field is changed. On the display device, there is the need to quickly go from displaying data for one color to displaying the next color. The color context switch affects both the light-on duty cycle and potentially color saturation. While the SIMD processor finishes displaying the prior color, data for the next color is being loaded in to the scratch memory in the periphery. Immediately upon the light turning off, the pixels are driven to an initial state (on or off) to ready them for the next color of light to be turned on.

With the fast TN LC and our context switch speed, we have achieved greater than 85% light on time with excellent color saturation.

2.4 Control High Speed Liquid Crystal
The LC switches to black in about 200 µS while the switch to white is about 600 µS. This asymmetry in the rise and fall time makes this material difficult if not impossible to control with digital drive methods that use multiple pulses drive [6]. Using on-display processing, we are able to generate a “single pulse” that would be impractical to support without on-display processing [4]. The drive algorithm has demonstrated good control of the LC over a wide range of temperatures without the need for calibration that would be required in multiple-pulse [6] methods.

Figure 4A shows our basic drive waveform at 50% light output. One thing to note is that the LC drives to white starts, if necessary, at the beginning of blanking. This lets the LC get to near full-on during the time of the context switch before the next color is turned on which helps with light efficiency. With single pulse drive, the output is inherently monotonic as the wider the pulse, the brighter the light output.

Figure 4B shows a representation of the problem with multi-pulse digital. The LC material response is a function of the rise and fall time of the LC material and the spacing of pulses. Mixes of pulses
of different widths are changed to affect the light output. Even small changes in the LC rise or fall time either due to process or by temperature can have significant effects on the monotonic response. A device with multiple pulses will likely require calibration whereas a single pulse can give very good results without calibration.

Figure 5 shows a series of pictures taken with the backplane cooled or heated to the temperatures indicated below each image. Even without any temperature compensation/adjustment, the light response remains monotonic.

3. Display Processing Architecture

Most other microdisplays built to date have little or no processing on the display device. Our device is different in that there is a massively parallel but simple processor built into the display device. There is a one-bit serial data path, known as the “processing element” or PE for each column of the display. The PE’s are controlled by a single controller that executes a program stored on the backplane.

Referring back to Figure 3, the processing is split in half with half the PE’s on the top and half the PE’s on the bottom of the display array.

The scratch SRAM on the top and bottom of the array is used to buffer pixel data being processed. Additionally, this scratch SRAM is used to buffer data used in making a “context switch” between to colors. The top PE’s control the top half of the pixels and the bottom PE’s the bottom half. The bit lines that go to the SRAM bits under the mirrors only have to run through about one-half of the display height which saves power. With PEs both on top and bottom, each PE drives one of two adjacent odd/even columns but on alternate cycles. A PE is therefore designed in the width of two pixels.

Figure 6 shows a block diagram of a single PE and its connection to the scratch memory and a mirror RAM column. Since PEs work bit-serially, the ALU and latches are each only one bit wide and a single PE has only a few dozen transistors. There is a latch on the output of the ALU that re-circulates intermediate results; this allows one of the ALU inputs to build up a multiple cycle result. The ALU in this implementation can perform 16 Boolean functions on the two inputs. These Boolean operations which have proven sufficient to perform the single pulse drive algorithms.

The scratch SRAM memory has about 3 bits per pixel but none of the bits are dedicated to any given pixel. The memory is constantly being re-allocated to different pixels based on proprietary algorithms that leverage the bit serial processing to reduce the number of processing cycles and to save power and the amount of storage required to minimize the SRAM in the periphery.

The on-display SIMD processor controls all the high speed operations on the display panel including
running a programmable algorithm and generating all the addresses to read the scratch RAM and the mirror memory as well as generating the control signals for the PE.

An external ASIC controller performs low speed control including the memory allocation on the panel. The ASIC also manages a single low power SDRAM that stores the image that is then sent to the panel field sequentially.

4. Field Rate and Programmable Field Width

The panel algorithm is soft loadable from flash and the panel is designed to support from 180 to 360 color fields per second. The various color fields can also vary in width to match the relative output characteristics of the various color light sources. The panel can also support so-called “white segments” where all 3 color light sources are turned on to boost light output with some loss in color saturation.

5. Backplane Technology

The CMOS silicon backplane was fabricated using a 0.18um 1.8V/5V process, and uses 5V transistors for the mirror RAM that drives the pixel and smaller 1.8V transistors for the rest of the SRAM and logic process. The technology could support smaller mirrors than a 5.4 µM implemented in this design. The CMOS technically used is very mature by semiconductor standards.

6. Resolution and Future Trends

Figure 7 shows a close up picture of an actual image projected by our display with 5.4µM pixels so that the individual mirrors/pixels can be seen. The text in the image has single pixel stroke fonts and note that the dots in the letter “i” and one pixel wide white space in-between the letters “m", "i", and “n” are clearly visible and well modulated. This also demonstrates that the pixels could be made smaller to support higher resolution with a small panel.

Anyone who has tried to browse normal (non-mobile) web pages or look at a file attachments on their PDA has come to realize the need for more resolution. Several cell phone manufacturers are already making mobile phones that have WVGA (~854x480 pixel) resolution displays and the expectation is that resolution requirement will keep increasing [1].

LCOS has advantages over other technologies in its scalability and in the low cost of developing new designs with different resolutions and mirror sizes. Since the mirrors/pixels are planar and don’t move, the gap between pixels can be very small which is important for eliminating the “screen door effects” and reducing the adverse effects of diffraction that can become significant with small pixels in other technologies. The mirrors can also be easily scaled up in size to match the étendue of light sources.

The current 854x600 LCOS device is being designed into both LED and Laser illuminated pico-projectors. LEDs currently have cost, size and simplicity advantages for lower brightness systems and are likely to be the illumination for most early pico-projectors.

Lasers, on the other hand, have made significant strides in cost and performance. They have significant advantages in terms of efficiency and brightness, particularly with small optics. Lasers and LCOS appear to be made for each other. The small étendue of lasers enables very small, yet high-resolution LCOS panels.

6. REFERENCES

http://techon.nikkeibp.co.jp/article/HONSHI/20080729/155633/